PTC-Based Sigma-Delta ADCs For High-Speed, Low-Noise Imagers

Adi Xhakoni, *Student Member, IEEE,*
Ha Le-Thai, Tomas Geurts, Genis Chapinal, and Georges Gielen, *Fellow, IEEE*

***Abstract*—This paper presents a novel column-parallel readout circuit for image sensors based on incremental-sigma-delta (ISD) ADCs. The excessive number of clock cycles needed per conversion is addressed. We apply the Photon Transfer Curve (PTC) based conversion to a second-order ISD ADC, achieving a 2.75x clock cycles reduction when compared to a standard second-order ISD ADC while maintaining the same noise performance. This results in the reduction of the pixel readout time and of the size of the digital filter.**

***Index Terms*—image sensor, low-noise, high frame rate, high resolution, ADC, Incremental $\Sigma\Delta$, Photon transfer curve**

I. Introduction

Low-light detection is a feature required in several imaging applications including scientific, surveillance, etc. Incremental sigma-delta ADCs have proven to be very effective in low-light detection [1][2][3] given their intrinsic oversampling while performing a single A/D conversion which reduces the thermal noise of the 4-Transistors [4] pixel source follower (SF). The state-of-the-art work with a column ISD ADC [3] achieves 1.9 electrons noise with 110 clock cycles per A/D conversion. The clock speed of ISD ADCs is normally below 50MHz. A higher clock speed increases the gain-bandwidth requirements of the opamps of the modulator, significantly increasing the power consumption.

This paper addresses the issue of the excessive number of clock cycles of conventional column-level ISD ADCs by applying the photon transfer curve based conversion method [4] to an ISD ADC.

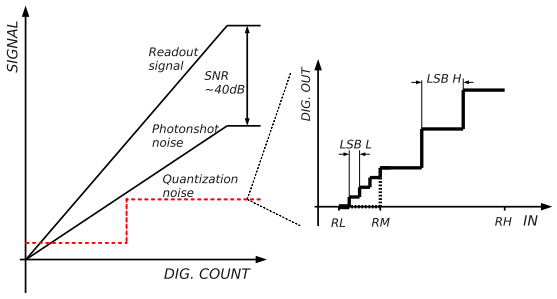

Fig. 1. Quantization step of a PTC-based ADC. Being the photon shot noise dominant at high light, a small quantization step is required only at low light.

A. Xhakoni, H. Le-Thai and G. Gielen are with the Department of Electrical Engineering ESAT-MICAS, KU Leuven, Leuven, Belgium e-mail: (adi.xhakoni@esat.kuleuven.be). T. Geurst and G. Chapinal are with ON Semiconductor, Mechelen, Belgium.

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II. Proposed column-parallel PTC-based ISD ADC

As the noise of the pixel at high light is dominated by the photon shot noise (Fig. 1), a high ADC resolution is needed only at low light [4] while at high-light levels it can be reduced, potentially saving power and reducing the conversion time.

Fig. 2 shows the simplified schematic of the proposed column readout architecture. The modulator is a standard second-order, feed-forward, single-bit architecture. As this topology is very tolerant to coefficient variations, a small 50fF capacitor is used as the sampling capacitor. A correlated-double-sampling (CDS) block ([5]) is placed in front of the ADC in order to shift the dark level of the pixel towards the common-mode voltage of the CDS. The resolution in bits N of the second order ISD is expressed as [3]:

$$N = log_2 M(M+1) - 1 \tag{1}$$

where M represents the number of clock cycles. According to (1) and considering that the input range of the ISD ADC depends on the DAC levels, the quantization step can be expressed as:

$$Qs = \frac{2(RH - RL)}{M(M+1)} \tag{2}$$

with RH and RL representing the DAC high and low reference voltages.

In the proposed architecture, the PTC-based quantization is obtained by adding an offset-compensated comparator and a third reference, RM, to the DAC of the modulator. The comparator detects if the ADC input signal is below a given threshold voltage. Depending on the comparison, RM (at low light) or RH (at high light) is chosen as the high DAC level with RL as fixed low level. We use RL=1V, RM=1.2V and RH=2.6V. According to (2), using RM instead of RH reduces the quantization step by 8x, corresponding to 3-bit low light extension. According to (1) and (2), 12-bit equivalent low-light ADC resolution can be achieved with 35 clock cycles. At high light, the resolution is 9-bit. As at high light the SNR of the pixel is limited by the photonshot noise to about 40dB, a 9-bit ADC is enough. Therefore, in an imager, this technique provides nearly the same performance of a conventional 12-bit ISD ADC while using less clock cycles.

To restore the conversion linearity between column ADCs using RH and those using RM, the output of the added comparator is stored as bit indicating the used reference. If RM is used, the LSB of the digital output of the ADC is mapped into the LSB of a 12-bit register. If RH is used, the

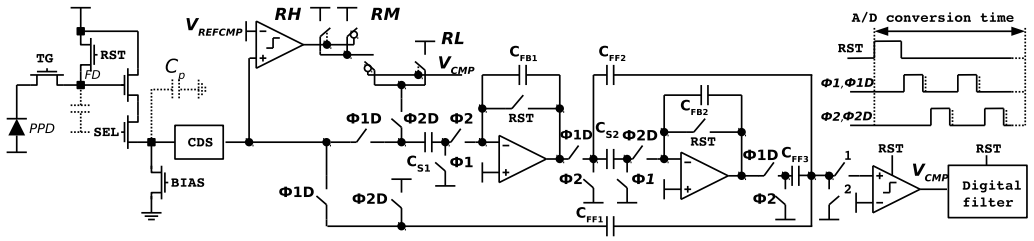

Fig. 2. PTC-based ISD ADC schematic and timing diagram. The modulator is a feed-forward second-order ISD ADC. The PTC conversion is achieved by adding a comparator and an extra DAC level, RM. The sampling capacitance of the ADC is 50fF while the gain of both integrators is 0.5.

MSB of the digital output of the ADC is mapped into the MSB of the 12-bit register.

Fig. 3 shows the simulated temporal noise at the output of the pixel SF at clock cycles ranging from 40 to 130. The noise is dominated by the ADC quantization noise therefore, the reduced clock cycles have little impact on the total temporal noise. Using as a benchmark the 110 clock cycles for 12-bit resolution of [3], to reach a similar noise we increase the number of clock cycles from 35 to 40, resulting in a 2.75x clock cycles reduction.

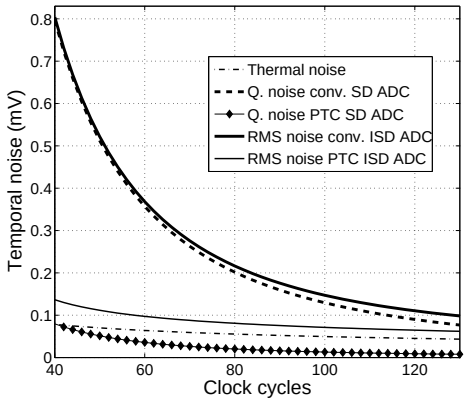

Fig. 3. Noise analysis of the signal path from pixel to ADC (Fig. 2) with the converter running in PTC and conventional mode at 20MHz clock speed and 50fF ADC sampling capacitance, in digital CDS mode. Being the quantization noise dominant over the pixel and ADC thermal noise, its reduction through the proposed PTD-based ADC is very effective in reducing the total temporal noise. The PTC-based ADC at 40 clock cycles has the same total temporal noise of a conventional ISD ADC running at 110 clock cycles.

III. Experimental results

The proposed column-parallel readout architecture has been applied to a 128 x 128, 10μm pitch, pixel array test chip in a 180nm CIS technology. Clocked at 20MHz with 40 clock cycles/conversion, it performs an A/D conversion in 2μs. The measured power consumption of each ADC is 200μW, dominated by the power-hungry folded-cascode amplifiers. These amplifiers were used for allowing different testing options. However, other opamp architectures such as common-source or telescopic amplifiers can be used, drastically reducing the power consumption. The measured noise and dynamic range are respectively 200μV and 77dB while the SNR at the switching point between RM and RH drops from 34.8db to 34.6dB, resulting in only 0.2dB SNR dip. As all the columns are subject to the same 3 reference voltages, no column-level calibration is needed. A sample image taken by the test chip is shown in Fig. 4.

Fig. 4. Raw image taken with 12 bit ADCs running in conventional mode with 110 samples (left) and in PTC mode with 40 samples (right) at 500fps. F=4.5. No difference is noted between the 2 modes confirming the validity of the proposed method.

IV. Conclusion

In this paper we have presented a PTC-based incremental sigma-delta ADC. Compared to the state-of-the-art ISD ADCs implementing the same modulator order, the proposed converter reduces the number of clock cycles by 2.75x while achieving a similar noise performance. The measured noise and dynamic range of the test chip with ISD ADCs using 40 clock cycles were respectively 200μV and 77dB, confirming the validity of the method. Column-level parallel readout architectures employing PTC-based ISD ADCs are valid candidates for low-noise, column-calibration-free imagers with high readout speed.

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